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NO. 1603 P. 6/11

MAR 08 2006

Ser. No. 10/830,019
Attorney Docket: 042264-0101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yoshiki KASHIWAGI et al.

Title: METHOD FOR DESIGNING
SEMICONDUCTOR CIRCUIT DEVICE,
UTILIZING BOUNDARY CELLS
BETWEEN FIRST AND SECOND CIRCUITS
DRIVEN BY DIFFERENT POWER SUPPLY
SYSTEMS
(as amended)

CERTIFICATE OF MAILING I hereby certify that this correspondence is being deposited via facsimile to ((571)) 273-8300 to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22312-1450, on the date below. Ruthie Vallejo (Printed Name) <i>Ruthie Vallejo</i> (Signature) March 8, 2006 (Date of Deposit)
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Appl. No.: 10/830,019

Filing Date: 04/23/2004

Examiner: To, Tuyen P.

Art Unit: 2825

SUPPLEMENTAL AMENDMENT AND REPLY UNDER 37 CFR 1.111

PLEASE ENTER

5 Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

10 Sir:

This communication is responsive to the Non-Final Office Action dated December 20, 2005, concerning the above-referenced patent application AND SUPPLEMENTAL TO THE REPLY MAILED MARCH 1, 2006.

Remarks/Arguments begin on page 5 of this document.

15 Please amend the application as follows: